EXHIBIT C

US 8,276,048 B2

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3. The system of claim **1**, wherein the determining is based on a latency requirement.

4. The system of claim **1**, wherein the determining is based on a bit error rate requirement.

5. A system that allocates shared memory comprising:

a transceiver that is capable of:

transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;

determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory;

allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

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allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and

deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

6. The system of claim **5**, wherein the determining is based on an impulse noise protection requirement.

7. The system of claim **5**, wherein the determining is based on a latency requirement.

8. The system of claim **5**, wherein the determining is based on a bit error rate requirement.

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